REMARKS

The Final Office Action mailed December 28, 2004, has been received and reviewed. Claims 1 through 12, 36 through 40, and 45 through 48 are currently pending in the application. Claims 1 through 12, 36 through 40, and 45 through 48 stand rejected. Applicants propose to amended claims 1, 4 through 9, 11, 12, 36 through 40 and 45 through 48, enter new claims 48 through 51, and respectfully request reconsideration of the application as proposed to be amended herein.

Responsiveness of Amendment Mailed Oct. 12, 2004.

The Examiner states that the Amendment mailed on Oct. 12, 2004, was not fully responsive because no arguments were presented pointing out the specific distinctions believed to render new claims 45 through 48 patentable over the applied references. However, Applicants submit that the Amendment mailed Oct. 12, 2004, was properly responsive as each of claims 45 through 48 depend from independent claims which were each argued to be patentable. As such, claims 45 through 48 were considered to define over the applied references at least be virtue of the distinctions pointed out for their respective base claims.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,498,099 to McLellan in view of U.S. Patent No. 6,255,740 to Tsuji

Claims 1 through 12, 36 through 40, and 45 through 48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McLellan (U.S. Patent No. 6,498,099 – hereinafter "McLellan") in view of Tsuji (U.S. Patent No. 6,255,740 – "hereinafter "Tsuji"). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of the claims are improper because the references relied upon fail to teach or suggest all of the limitations of the presently claimed invention.

Claims 1 through 11 and 45

Independent claim 1, as proposed to be amended herein, is directed to a method of fabricating an integrated circuit package. The method comprises: providing a semiconductor die having a plurality of bond pads on an active surface thereof; providing a lead frame *including a plurality of discretely defined conductive leads*; electrically coupling a first bond pad of the plurality of bond pads to a first portion of a first discretely defined conductive lead of the plurality of conductive leads; *electrically coupling a second bond pad of the plurality of bond pads to a second portion of the first discretely defined conductive lead*; and *electrically isolating the first portion of the first discretely defined conductive lead from the second portion of the first discretely defined conductive lead.*

The Examiner cites McLellan as disclosing a method of fabricating an integrated circuit package, wherein the method comprises: "providing a semiconductor die 206 having a plurality of bonds on an active surface thereof; providing a lead frame 100 including a plurality of conductive leads 203, electrically coupling 205 a first bond of the plurality of bonds to a first portion of the at least one conductive lead of the plurality of conductive leads, electrically coupling a second bond of the plurality of bonds to a second portion of the at least one conductive lead; and electrically isolating the first portion of the at least one conductive lead from the second portion of the at least one conductive lead; and inherently disposing a volume of electrically insulating material (air) between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion..." (Final Action page 4).

The Examiner states that McLellan doesn't explicitly disclose disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion. However, the Examiner cites Tsuji as disclosing such subject matter stating that it would be obvious to combine McLellan and Tsuji to "protect the package of McLellan." (Final Action, pages 9 and 10). Applicants respectfully traverse the rejection of claim 1.

McLellan discloses a method of forming a leadless plastic chip carrier by partial etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined, in part, by the half etching process and then wire-bonded to a semiconductor die. The leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the "copper panel substrate." (See, e.g., col. 3, lines 9-56). However, McLellan does not teach or suggest providing a lead frame including a plurality of *discretely defined conductive leads*, electrically coupling a first bond pad of the plurality of bond pads to a first portion of a first discretely defined conductive lead of the plurality of conductive leads, electrically coupling a second bond pad of the plurality of bond pads *to a second portion of the first discretely defined conductive lead* , (or in other words, coupling two different bond pads with the *same discretely defined conductive lead*) and then electrically isolating the first portion of the first discretely defined conductive lead from the second portion of the first discretely defined conductive lead.

Applicants submit that McLellan simply does not teach or suggest coupling two different bond pads of a semiconductor die to first and second portions of the same discretely defined conductive lead and electrically isolating the first and second portion from one another. Rather, McLellan teaches that a "copper panel is provided, to which photoresist 502 is applied and patterned for a 'first level' connect (FIG. 5B)." (Col. 4, lines 13-15). Additionally, portions of the copper panel are plated with Cu/Ni/Al to defined contact pads (203) and an attach pad (202) on the upper surface of the copper panel. (See, col. 4, lines 15-19). A similar process is repeated to define contact pad and attach pad "protrusions" on the bottom surface of the copper panel.

(See, col. 4, lines 20-25). After the semiconductor (206) is attached to the attach pad (202) and is wire bonded to the contact pads, a final etch back is performed, as shown in FIG. 5I, so as to separate individual contact pads defined on the copper substrate. Thus, Applicants submit that McLellan fails to teach or suggest that two different bond pads of a semiconductor die are coupled to a single discretely defined conductive lead. Rather, each discretely defined conductive lead or contact pad (203) appears to have only a single bond pad coupled therewith (as indicated by single wire bonds in the drawings).

Applicants further submit that Tsuji fails to teach or suggest such subject matter. Indeed, referring to FIG. 4A and FIG. 4B, Tsuji appears to disclose that each bond pad (41a) is coupled with a separate and discrete trace of the pattern layer (32) of a printed wiring board. (See, e.g., col. 9, lines 49-53; col. 10, lines 31-33; FIGS. 4A, 4B).

Applicants, therefore, submit that claim 1 is clearly patentable over the combination of McLellan and Tsuji. Applicants further submit that claims 2 through 11 and 45 are also allowable at least be virtue of their dependency from an allowable base claim.

With respect to claim 45, Applicants note that the Examiner states that it would have been an obvious matter of design choice to choose a particular angle at which the leads extend from a peripheral edge of a die paddle and that the angle is for a nonobvious purpose. However, as indicated in the specification of the present application, configuring the leads to exhibit such an angle provides advantages at least for purposes of wire bonding patterns and processes (see, e.g., as-filed application, paragraph [0033]), and the Examiner has not cited McLellan or Tsuji as teaching or suggesting such subject matter.

Applicants, therefore, respectfully request reconsideration and allowance of claims 1 through 11 and 45.

Claims 12 and 46

Independent claim 12, as proposed to be amended herein, is directed to a method of forming an array of electrically conductive elements on an integrated circuit package. The method comprises: securing a semiconductor die having a plurality of bond pads on an active surface thereof to a lead frame having a plurality of *discretely defined leads*; electrically coupling

at least *two spaced locations of each discretely defined lead of the plurality of discretely defined leads with at least two different bond pads of the plurality of bond pads*; and *severing each lead between the at least two spaced locations to form at least two electrically isolated conductive elements.*

The Examiner cites McLellan as teaching a method of forming an array of electrically conductive elements on an integrated circuit package wherein the method comprises: "securing a semiconductor die having a plurality of bonds on an active surface thereof to a lead frame having a plurality of leads; electrically coupling each lead of the plurality of leads at spaced locations with one of at least two different bonds of the plurality of bonds; severing each lead between the spaced locations to form at least two electrically isolated conductive elements; and inherently disposing an electrically insulative material (air) between the at least two spaced location of each lead subsequent the severing..." (Final Action, page 6).

The Examiner states that McLellan doesn't explicitly disclose disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the first portion from the second portion. However, the Examiner cites Tsuji as disclosing such subject matter stating that it would be obvious to combine McLellan and Tsuji to "protect the package of McLellan." (Final Action, pages 9 and 10). Applicants respectfully traverse the rejection of claim 12.

McLellan discloses a method of forming a leadless plastic chip carrier by partial etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined, in part, by the half etching process and then wire-bonded to a semiconductor die. The leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the "copper panel substrate." (See, e.g., col. 3, lines 9-56). However, McLellan does not teach or suggest providing a lead frame including a plurality of *discretely defined conductive leads*, electrically coupling a first bond pad of the plurality of bond pads to a first portion of a first discretely defined conductive lead of the plurality of conductive leads,

electrically coupling a second bond pad of the plurality of bond pads *to a second portion of the first discretely defined conductive lead* , (or in other words, coupling two different bond pads with the *same discretely defined conductive lead*) and then electrically isolating the first portion of the first discretely defined conductive lead from the second portion of the first discretely defined conductive lead.

Applicants submit that McLellan simply does not teach or suggest coupling two different bond pads of a semiconductor die to first and second portions of the same discretely defined conductive lead and electrically isolating the first and second portion from one another. Rather, McLellan teaches that a "copper panel is provided, to which photoresist 502 is applied and patterned for a 'first level' connect (FIG. 5B)." (Col. 4, lines 13-15). Additionally, portions of the copper panel are plated with Cu/Ni/Al to defined contact pads (203) and an attach pad (202) on the upper surface of the copper panel. (See, col. 4, lines 15-19). A similar process is repeated to define contact pad and attach pad "protrusions" on the bottom surface of the copper panel. (See, col. 4, lines 20-25). After the semiconductor (206) is attached to the attach pad (202) and is wire bonded to the contact pads, a final etch back is performed, as shown in FIG. 5I, so as to separate individual contact pads defined on the copper substrate. Thus, Applicants submit that McLellan fails to teach or suggest that two different bond pads of a semiconductor die are coupled to the same discretely defined conductive lead. Rather, each discretely defined conductive lead or contact pad (203) appears to have only a single bond pad coupled therewith (as indicated by single wire bonds in the drawings).

Applicants further submit that Tsuji fails to teach or suggest such subject matter. Indeed, referring to FIG. 4A and FIG. 4B, Tsuji appears to disclose that each bond pad (41a) is coupled with a separate and discrete trace of the pattern layer (32) of a printed wiring board. (See, e.g., col. 9, lines 49-53; col. 10, lines 31-33; FIGS. 4A, 4B).

Applicants, therefore, submit that claim 12 is clearly patentable over the combination of McLellan and Tsuji. Applicants further submit that claim 46 are also allowable at least be virtue of their dependency from an allowable base claim.

With respect to claim 46, Applicants note that the Examiner states that it would have been an obvious matter of design choice to choose a particular angle at which the leads extend

from a peripheral edge of a die paddle and that the angle is for a nonobvious purpose. However, as indicated in the specification of the present application, configuring the leads to exhibit such an angle provides advantages at least for purposes of wire bonding patterns and processes (see, e.g., as-filed application, paragraph [0033]), and the Examiner has not cited McLellan or Tsuji as teaching or suggesting such subject matter.

Applicants, therefore, respectfully request reconsideration and allowance of claims 12 and 46.

Claims 36 through 40, 47 and 48

Independent claim 36, as amended herein, is directed to a method of fabricating a semiconductor die assembly. The method comprises: placing a semiconductor die within a plurality of discretely defined leads extending laterally outwardly from peripheral edges thereof; *wire bonding at least two bond pads of a plurality of bond pads on the semiconductor die to at least two spaced locations on each of the discretely defined leads of the plurality*; transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and the plurality of discretely defined leads, leaving undersurfaces of the plurality of discretely defined leads exposed; and *severing each of the plurality of discretely defined leads between each of the at least two spaced locations*.

The Examiner cites McLellan as disclosing a method of fabricating a semiconductor die assembly wherein the method comprises: "placing a semiconductor die within a plurality of leads extending laterally outwardly form peripheral edges thereof; wire bonding bonds on the semiconductor die to spaced locations on the leads of the plurality; transfer molding a dielectric encapsulant over the semiconductor die, wire bonds and leads, leaving the undersurfaces of the leads exposed; severing the leads between the spaced locations; and inherently disposing a volume of electrically insulative material between the spaced locations subsequent severing each of the plurality of leads..." (Final Action, pages 6 and 7).

The Examiner states that McLellan doesn't explicitly disclose disposing a volume of electrically insulating material between the first portion of the at least one conductive lead and the second portion of the at least one conductive lead subsequent the electrically isolating the

first portion from the second portion. However, the Examiner cites Tsuji as disclosing such subject matter stating that it would be obvious to combine McLellan and Tsuji to "protect the package of McLellan." (Final Action, pages 9 and 10). Applicants respectfully traverse the rejection of claim 36.

McLellan discloses a method of forming a leadless plastic chip carrier by partial etching one or both sides of the package design or pattern onto a leadframe strip. Contact pads (203) are defined, in part, by the half etching process and then wire-bonded to a semiconductor die. The leadframe (100) and semiconductor die (206) are molded within a plastic or epoxy material. Subsequent the molding operation, the leadframe is further etched to isolate the contact pads from other components of the "copper panel substrate." (See, e.g., col. 3, lines 9-56). However, McLellan does not teach or suggest providing a lead frame including a plurality of *discretely defined conductive leads*, electrically coupling a first bond pad of the plurality of bond pads to a first portion of a first discretely defined conductive lead of the plurality of conductive leads, electrically coupling a second bond pad of the plurality of bond pads *to a second portion of the first discretely defined conductive lead* , (or in other words, coupling two different bond pads with the *same discretely defined conductive lead*) and then electrically isolating the first portion of the first discretely defined conductive lead from the second portion of the first discretely defined conductive lead.

Applicants submit that McLellan simply does not teach or suggest coupling two different bond pads of a semiconductor die to first and second portions of the same discretely defined conductive lead and electrically isolating the first and second portion from one another. Rather, McLellan teaches that a "copper panel is provided, to which photoresist 502 is applied and patterned for a 'first level' connect (FIG. 5B)." (Col. 4, lines 13-15). Additionally, portions of the copper panel are plated with Cu/Ni/Al to defined contact pads (203) and an attach pad (202) on the upper surface of the copper panel. (See, col. 4, lines 15-19). A similar process is repeated to define contact pad and attach pad "protrusions" on the bottom surface of the copper panel. (See, col. 4, lines 20-25). After the semiconductor (206) is attached to the attach pad (202) and is wire bonded to the contact pads, a final etch back is performed as shown in FIG. 5I so as to separate individual contact pads defined on the copper substrate. Thus, Applicants submit that

McLellan fails to teach or suggest that two different bond pads of a semiconductor die are coupled to the same discretely defined conductive lead. Rather, each discretely defined conductive lead or contact pad (203) appears to have only a single bond pad coupled therewith (as indicated by single wire bonds in the drawings).

Applicants further submit that Tsuji fails to teach or suggest such subject matter. Indeed, referring to FIG. 4A and FIG. 4B, Tsuji appears to disclose that each bond pad (41a) is coupled with a separate and discrete trace of the pattern layer (32) of a printed wiring board. (See, e.g., col. 9, lines 49-53; col. 10, lines 31-33; FIGS. 4A, 4B).

Applicants, therefore, submit that claim 36 is clearly patentable over the combination of McLellan and Tsuji. Applicants further submit that claim 37 through 40, 47 and 48 are also allowable at least be virtue of their dependency from an allowable base claim.

With respect to claim 47, Applicants note that the Examiner states that it would have been an obvious matter of design choice to choose a particular angle at which the leads extend from a peripheral edge of a die paddle and that the angle is for a nonobvious purpose. However, as indicated in the specification of the present application, configuring the leads to exhibit such an angle provides advantages at least for purposes of wire bonding patterns and processes (see, e.g., as-filed application, paragraph [0033]), and the Examiner has not cited McLellan or Tsuji as teaching or suggesting such subject matter.

Applicants, therefore, respectfully request reconsideration and allowance of claims 36 thorough 40, 47 and 48.

ENTRY OF AMENDMENTS

The amendments to claims 1, 4 through 9, 11, 12, 36 through 40 and 45 through 48 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

ENTRY OF NEW CLAIMS

New claims 49 through 51 above should be entered by the Examiner because they are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, Applicant submits that the new claims do not raise new issues or require a further search.

Applicants also submit that claims 49 through 51 are allowable at least by virtue of their respective dependency from allowable base claims.

New claim 49 includes the subject matter of defining a concavity between the first portion and second portion of the discretely defined leads, and forming a structural member in the concavity including filling the concavity with a volume of electrically insulating material. Applicants submit that the references relied upon fail to teach or suggest such subject matter.

New claim 50 includes the subject matter of defining a concavity between the two spaced locations and forming a structural member in the concavity including filling the concavity with a volume of electrically insulating material. Applicants submit that the references relied upon fail to teach or suggest such subject matter.

New claim 51 includes the subject matter of defining a concavity between the at least two spaced locations and forming a structural member in the concavity including filling the concavity with a volume of electrically insulating material. Applicants submit that the references relied upon fail to teach or suggest such subject matter.

CONCLUSION

Claims 1 through 12, 36 through 40, and 45 through 51 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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